WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

an element isolation region provided in the semiconductor substrate and including a thick element isolating insulation film, for isolating an element region;

a first gate electrode provided on the element region in the semiconductor substrate in self-alignment with the element isolation region;

a second gate electrode provided on the first gate electrode with an insulation film interposed therebetween; and

a resistance element provided on the element isolation region, the resistance element and the second gate electrode being formed of a same conductive film.

2. The semiconductor memory device according to claim 1, further comprising an impurity diffusion layer formed in a surface of the semiconductor substrate and surrounding a region corresponding to the resistance element, the impurity diffusion layer having a conductivity type which is equal to that of the semiconductor substrate and an impurity concentration which is higher than that of the semiconductor substrate.

3. The semiconductor memory device according to claim 1, wherein the first gate electrode is a floating

gate electrode of a nonvolatile semiconductor memory, and the second gate electrode is a control gate electrode.

4. The semiconductor memory device according to claim 1, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

5. The semiconductor memory device according to claim 2, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

6. A semiconductor memory device comprising:

a semiconductor substrate;

an element isolation region provided in the semiconductor substrate and including a thick element isolating insulation film, for isolating an element region; and

a resistance element provided on the element isolation region and formed of a conductive film,

wherein the semiconductor substrate has impurity concentration profile which is set to be constant or be lower in accordance with the depth of the semiconductor substrate getting shallower toward the region corresponding to the resistance element.

7. The semiconductor memory device according to claim 6, further comprising an impurity diffusion layer formed in a surface of the semiconductor substrate and

surrounding a region corresponding to the resistance element, the impurity diffusion layer having a conductivity type which is equal to that of the semiconductor substrate and an impurity concentration which is higher than that of the semiconductor substrate.

8. The semiconductor memory device according to claim 6, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

9. The semiconductor memory device according to claim 7, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

10. A semiconductor memory device comprising:

a semiconductor substrate of a first conductivity type;

an element isolation region provided in the semiconductor substrate, for isolating an element region;

a resistance element provided on the element isolation region and formed of a conductive film; and

an opposite-conductivity-type diffusion layer of a second conductivity type that is opposite to the first conductivity type of the semiconductor substrate, the opposite-conductivity-type diffusion layer being formed in the element region adjacent to the element

isolation region on which the resistance element is provided.

11. The semiconductor memory device according to claim 10, wherein a positive voltage is applied to the resistance element and the opposite-conductivity-type diffusion layer when the semiconductor substrate is a P type and a negative voltage is applied to the resistance element and the opposite-conductivity-type diffusion layer when the semiconductor substrate is an N type.

12. The semiconductor memory device according to claim 10, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

13. The semiconductor memory device according to claim 11, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

14. A method of manufacturing a semiconductor memory device, comprising the steps of:

forming a gate oxide film and a first conductive film on a memory cell array region and a peripheral circuit region of a semiconductor substrate;

forming a mask material on the first conductive film where the cell transistor is to be formed in the memory cell array region;

forming trenches by etching the first conductive

film and the gate oxide film with the mask material;

forming an insulation film in the trenches in the memory cell array region and the peripheral circuit region;

removing the mask material;

forming a first insulation film on at least the first conductive film;

forming a second conductive film on the first insulation film in the memory cell array region and the peripheral circuit region; and

forming the resistance element by etching the second conductive film on the peripheral region.

15. The method of manufacturing a semiconductor memory device according to claim 14, wherein the second conductive film serves as a control gate of the cell transistor in the memory cell array region and serves as the resistance element in the peripheral region.